

Maltepe University
Department of Electronics Engineering
Digital Electronics (ELK 204)

GENERAL COURSE INFORMATION

Instructor : Asst. Prof. Dr. Mehmet SAĞBAŞ
Office : MUH 314
Office Hours : Monday: 12.10-13.00, Tuesday: 14.00-14.50, Friday: 14.00-14.50
Campus Phone : 0216 626 10 50 / 1839
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Class Times and : Theory:
Classroom Monday: 11.10-12.00 (308); Thursday: 10.10-11.00 (308); Friday:
11.10-12.00 (309)
Laboratory:
Thursday: 09.10-11.00 (Electronics Lab)
Text Book : M. MORRIS MANO, "SAYISAL TASARIM", Translation of Digital
Design 2nd Ed. into Turkish, Literatür Publication, İstanbul, 2003.
ISBN: 975-8431-29-3

LECTURE OUTLINES

<u>Part</u>	<u>Lecture</u>
1	Binary Systems <ul style="list-style-type: none">• Digital computers and digital systems• Binary numbers• Number base conversions• Octal and hexadecimal numbers• Complements• Signed binary numbers• Binary codes• Binary storage and registers• Binary logic

- 2 Boolean Algebra and Logic Gates**
- Basic definitions
 - Axiomatic definition of Boolean algebra
 - Basic theorems properties of Boolean algebra
 - Boolean functions
 - Canonical and standard forms
 - Other logic operations
 - Digital logic gates
 - Integrated circuits
- 3 Simplification of Boolean Functions**
- The map method
 - Two-and three-variable maps
 - Four variable maps
 - Five variable maps
 - Product of sum simplification
 - NAND and NOR implementations
 - Other two level implementations
 - Don't-care conditions
 - Determination of prime implicants
 - Selection of prime implicants
- 4 Combinational Logic**
- Introduction
 - Design procedure
 - Adders
 - Subtractors
 - Code conversion
 - Analysis procedure
 - Multilevel NAND circuits
 - Multilevel NOR circuits
 - Exclusive-OR functions
- 5 MSI Components**
- Introduction
 - Binary adder and subtractor
 - Decimal adder
 - Magnitude comparator
 - Decoders and encoders
 - Multiplexes
- 6 Synchronous Sequential Logic**
- Introduction
 - Flip-flops
 - Triggering of flip-flops

- Analysis of clocked sequential circuits
- State reduction and assignment
- Flip-flop excitation tables
- Design procedure
- Design of counters

7 Registers, Counters, and the Memory

- Introduction
- Registers
- Shift registers
- Ripple counters
- Synchronous counters
- Timing sequences

HOMWORK

Homework must be neatly prepared and should be submitted in time. Late homework will not be accepted. Effect of homework to the overall grade will be 10%.

ATTENDANCE and PARTICIPATION

- It is obligatory to attend the classes. Students should be in class on time.
- Students are expected to raise questions and participate in class discussions.
- To be able to attend the final exam, students must succeed (laboratory grade ≥ 50) in the laboratory.

Students should attend, at least, 70% (80%) of the classes (tutorials and/or labs). Otherwise, they will not be given permission to take the exams.

GRADING

Grading will be as follows:

Midterm Exam : 19 % [10th Academic Week]

Homework and Quiz : 1 % at least 5.

Laboratory : 20 %

Final : 60 %